

Bulk materials that, when they degrade, release or discharge nanomaterials can be clearly identified, regulated and controlled, as necessary, without being defined themselves as nanomaterials (e.g. regulations limiting the presence of certain hazardous materials in electronics distinguish between the hazardous substances of interest and the equipment within which they may be found).

It is the distinction between the material of interest and other materials that they may contain that allows industry and government to define more precisely what they want to control and regulate.

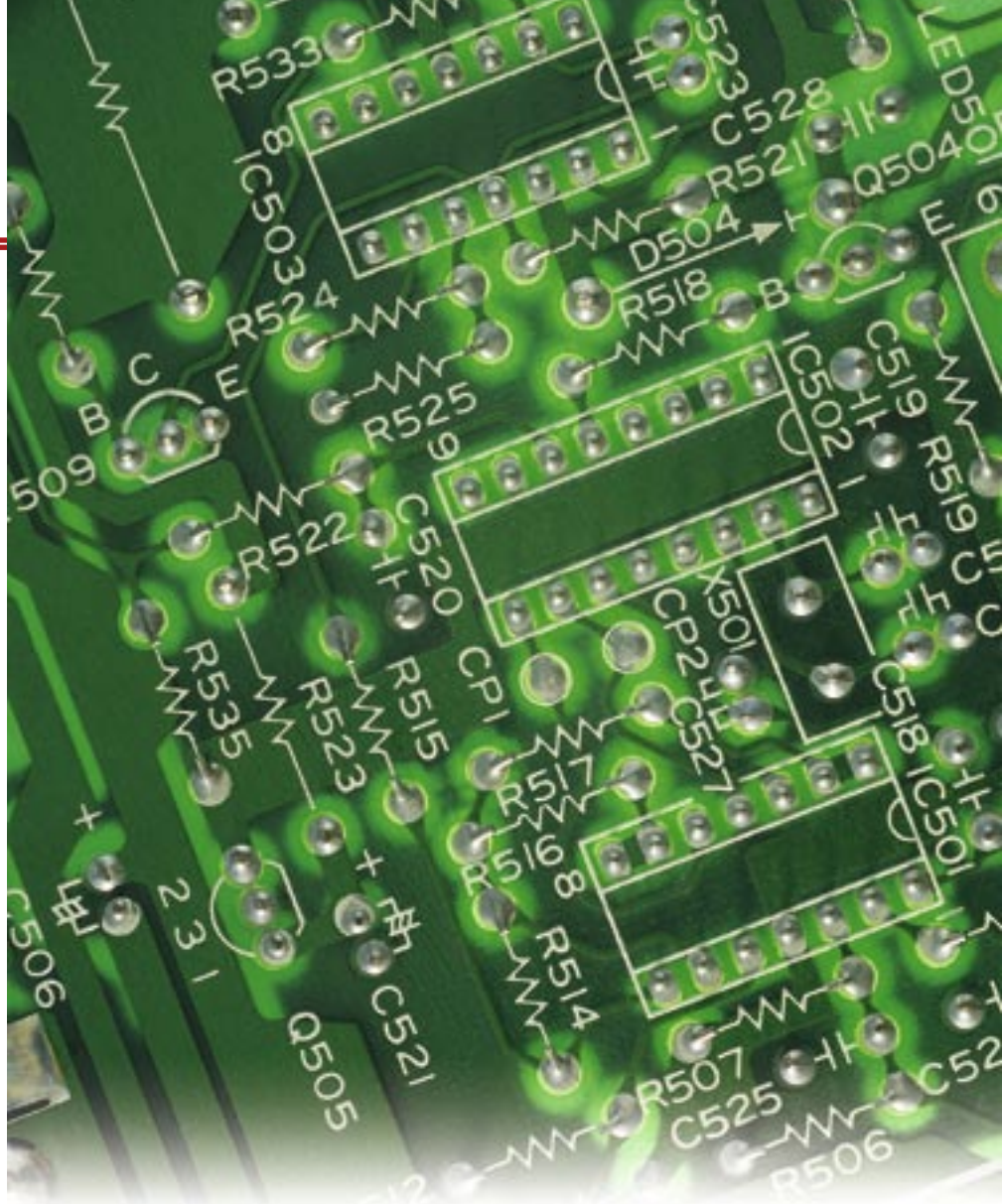
### Managing the terminology output

In most cases, the development of standard consensus-based definitions and terminology is derived from a broad usage in scientific and trade literature and the ISO process will draw on existing scientific usage to the extent possible in developing definitions and terminology for nanotechnology.

However, it is relatively early in the development of the field and, as already mentioned, relatively few nanoproducts are on the market. This will require nanotechnology definitions and terminology to evolve as the domain moves towards its full potential. Achieving this dynamic management regime for the definitions and terminology will require efforts outside the normal practices of ISO.

New definitions must be developed regularly and as required during this evolutionary phase, and these will then need to be embedded in the terminology and linked, as appropriate, to other existing standards.

The terminology for nanotechnologies will require ongoing management as it expands and matures over the next decade or so. While it is early to define the nature of such administration, it will be important to recognize these requirements as the definitions and the terminology structure are developed and to incorporate tactics for managing this growth within the ISO process. ■



## Sustaining Moore's Law – Microelectronics, nanoelectronics and beyond

by Dr. Paolo A. Gargini,  
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**M**ore than 30 years after Intel founder Gordon Moore predicted a doubling in semiconductor capacity approximately every 24 months, transistor density on silicon chips continues to increase at about that rate.

As the physical limits of miniaturization are reached in coming years, nanoelectronics will pave the way for continued gains.

### The electronic revolution

John Fleming invented the electronic diode vacuum tube in 1904, and two years later Lee DeForest invented the triode vacuum tube.

By 1950, about 500 million electron vacuum tubes per year were sold.

Julius Edgar Lilienfeld filed three patents between 1925 and 1928 that clearly stated the concept and application of field effect transistors.

The first serious attempt to realize a solid state field effect device began in the summer of 1945 at the Bell Labs under the leadership of William Shockley.

The group decided to concentrate on crystals of silicon and germanium to realize the field effect transistor conceived by Lilienfeld.

Finally, after a number of experiments, the group succeeded in interposing a gold contact between two point contacts on the surface of a germanium sample, and by applying a positive bias to the gold and a negative bias to the adjacent contact, he demonstrated

the necessary voltage gain in December 1947.

By early 1948 the junction transistor theorized by Shockley was demonstrated.

Together with his colleagues Walter Brattain and John Bardeen, Shockley was awarded the Nobel Prize in 1956 for the invention of the transistor.

Shockley left Bell Labs and established the Shockley Semiconductor Laboratory (SSL) in 1955 with the goal of commercializing novel semiconductor devices.

### Walter Brattain, John Bardeen, William Shockley were awarded the Nobel Prize in 1956

By September 1957, Gordon Moore and Robert Noyce left SST with six other scientists to found Fairchild Semiconductors.

By 1959 both Jack Kilby and Robert Noyce had invented the integrated circuit by using gold wires and aluminium metallization respectively demonstrating that aluminium made good contacts to both p-type and n-type silicon.

The technology arsenal was completed and finally by the mid-1960s the development of the first metal-oxide-semiconductor (MOS) devices made by the self-aligned silicon gate process was demonstrated.

### About the author



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### Moore's Law

In 1965 Gordon Moore predicted that the number of transistors per chip would double every year for at least 10 years or so. In 1975 he updated his prediction to once every two years.

In an article published on 19 April 1965 celebrating the 35<sup>th</sup> anniversary of *Electronics Magazine*, Moore stated: "With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65 000 components on a single silicon chip." The highest level of integration obtained in 1965 was about 64 components on a chip.

Noyce and Moore understood that the commercially successful technology had finally arrived and founded Intel Corporation in 1968, just as demand began to grow for various types of memory modules.

Finally, in 1974, Robert Dennard of IBM published the famous theory of scaling which provided the key to rapidly predict how to design MOS devices from one generation to the next in accordance to a well-defined set of rules.

In December 1975, Moore readjusted his forecast: "I see no reason to expect the rate of progress in the use of smaller dimensions in complex circuits to decrease in the near future. With respect to the factor contributed by devices and circuit cleverness however, the situation is different. We are approaching a limit that must slow the rate of progress. The new slope might approximate a doubling every two years."

Gordon Moore's predictions still stand after more than 40 years.

### The microelectronics era

In the subsequent years, each new generation of process technology was expected to reduce minimum feature size by approximately a factor of 0.7.

That reduction in linear feature size was generally considered to be a worthwhile step to take for a new process generation, as it provided roughly a doubling increase in transistor density.

During the 1970s and 1980s, the semiconductor industry was introducing new technology generations for DRAM memory devices approximately every three years.

The contribution of scaling translated into a doubling in transistor density every three years, but by means of memory cell optimization and by means of increasing chip size, quadrupling in the number of transistors every 3 years was accomplished.

On the other hand, microprocessors maintained a more even pace, doubling in transistors about every two years. By the mid-1990s, it became impossible for DRAM to cost-effectively further increase chip size and DRAM and microprocessors have improved at about the same rate since (i.e. doubling transistors count every two years).

The basic materials of the field effect device in the 1960s were aluminium, silicon dioxide and silicon substrate from which the transistors first became known as metal-oxide-semiconductors, or MOS.

Polycrystalline silicon became the dominant gate electrode material in the 1970s, to be augmented by tungsten silicide and subsequently by titanium silicide in the 1980s.

These materials evolved into cobalt and nickel silicide in the 1990s while aluminium began to be replaced by copper at the turn of the century due its lower resistivity.

### Nanoelectronics

From the feature size for individual transistors of approximately 10 micron in the late 1960s, the semiconductor industry crossed the 1 micron (millionth of a metre) feature mark around 1986.

MOS devices with minimum dimensions below 100 nm (billionth of a

## Main Focus

metre) were first produced and shipped to the marketplace around the year 2000, marking the beginning of the nanoelectronics era for the semiconductor industry.

As transistor scaling entered into the 21<sup>st</sup> century, several fundamental problems needed to be solved.

Gate oxide defects have been reduced to such a low level that current oxide leakage can be exclusively attributed to the quantistic effect of tunneling.

However, as the thickness of the insulating oxide film continues to be reduced, it will be impossible to further scale down below three to four atomic layers.

Excellent results have been reported by replacing silicon dioxide with an insulator with higher dielectric constant.

Recently, Mark Bohr, Intel Senior Fellow, announced an historical breakthrough: "After 40 years from the invention of the silicon gate MOS transistor, Intel researchers have developed record-setting, high-performance transistors using a new material, called high-k, for the gate dielectric and new metal materials for the transistor gate."

As transistor dimensions continue to scale down, the number of the implanted atoms in the channel to control threshold voltage is reduced to only a few.

By replacing the gate electrode with appropriate metal gates, it is possible also to control the threshold voltage without using any ion implantations as the work function of the metal will determine the threshold voltage.

Mobility degradation has been observed in conjunction with aggressively scaling MOS transistors. Recent results indicate that mobility enhancement has been obtained by manipulating the silicon lattice spacing by locally induced stress.

In addition, use of materials such as germanium, with an intrinsic mobility about three times that of sili-

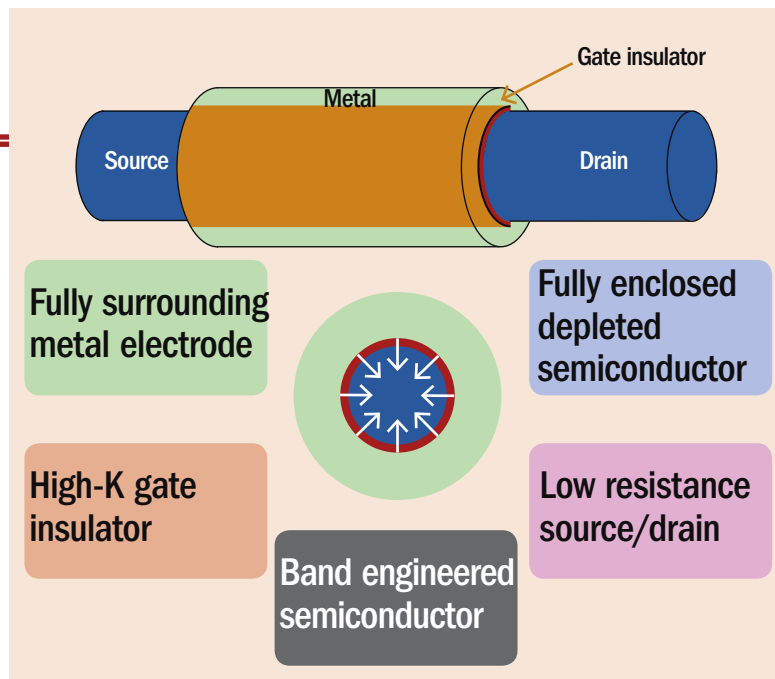


Figure 1 – The ideal MOS transistor.

con, promises to further increase channel mobility.

Direct source to drain tunneling is considered the ultimate electric limiter for the field-effect transistor. It appears that the smallest possible distance between the source and drain regions is about 5 nm.

This limit will not be approached until approximately the year 2020, and Moore's Law is expected to hold until then.

### ...And beyond

But this is not the end of the story. The electron current-based devices now in use only utilize the attributes of mass and charge.

Other state variables such as spin, wave function amplitude and wave function phase have been proposed as the foundation of new devices to augment and/or replace the Free Evolutionary Timetabling software (FET) devices in the future.

The search for a potential new device, to be available by 2020, needs to be initiated now. Rather than replacing MOS devices, this new device will likely work in conjunction with them, marking the beginning of convergence between nanotechnology and the first elements of the vision outlined by Richard Feynman in his seminal 1959 talk predicting the rise of nanotechnology entitled "There's Plenty of Room at the Bottom".

These elements, if appropriately melded together, will represent the foundation of the picotechnology that

will take us to the middle of the 21<sup>st</sup> century.

Only by constructing a strong cooperation among physics, chemistry and biology will the new engineering community be able to identify the manufacturable solutions that will power the world-changing products yet to be envisioned.

### The contribution of standardization

Standardization has been critical in supporting the market development of the semiconductor industry which has made these dramatic advances possible.

International Standards developed by SEMI (Semiconductor Equipment and Materials International) and its partners (i.e. ASTM, DIN, IEEE, ISO and JEITA) have supported improvement in production and quality control of the raw material, primarily silicon, where defect-free crystals have increased in diameter from one or two centimetres in diameter in the early years to over 300 millimetres today.

But standards also apply to the conversion of raw material into planar substrates by cutting and chemo-mechanical polishing (examples of relevant standards are the ISO 13565 series, *Geometrical Product Specifications (GPS) Surface texture: Profile method; Surfaces having stratified functional properties*) and to the design and operation of the FABS (Fabrication facilities) where the devices are manufactured. As device sizes have become smaller, the acceptable levels of contamination, both chemical and particulate, have had to be reduced to vanishingly small levels, e.g. the ultra-clean areas of modern FABS that operate at ISO Class 1 (less than 1 particle exceeding 0.5 micron per cubic metre – as specified in the ISO 14644 standards series, *Cleanrooms and associated controlled environments*).

It is expected that standards will also play a major role in the nanotechnology era as new and diverse materials and fabrications techniques are introduced into the semiconductor industry. ■